In the Claims:

On page 14, cancel line 1, and substitute the following left-hand justified heading therefor:

--**I Claim As My Invention:**--.

Please cancel claims 1-9, without prejudice, and substitute the following claims therefor:

10. An integrated circuit, comprising:

a plurality of logic gates for implementing a logic function of the integrated circuit; and

a self-test circuit for performing an internal self test of the plurality of logic gates, the self-test circuit including a test pattern generator for generating a test pattern, a test response analyzer for evaluating a test response, and an input/output circuit via which the self-test circuit further performs a logic test of an external circuit, the self-test circuit testing both the plurality of logic gates and the external circuit at the same time, wherein a first part of the test pattern is supplied to the plurality of logic gates and a second part of the test pattern is supplied to the external circuit via the input/output circuit, and the test response is produced from a first part of the test response from the plurality of logic gates and a second part of the test response from the external logic circuit.

11. An integrated circuit as claimed in claim 10, wherein both the test pattern generator and the test response analyzer are linear-feedback shipped registers.

12. An integrated circuit as claimed in claim 10, wherein the test pattern generator generates pseudo-random vectors as the test pattern.

13. An integrated circuit as claimed in claim 10, wherein the input/output circuit includes input/output drivers for sending and receiving unidirectional signals between the self-test circuit and the external circuit.

14. An integrated circuit as claimed in claim 10, wherein the input/output circuit includes controllable input/output drivers for sending and receiving bidirectional signals between the self-test circuit and the external circuit, and wherein the self-test circuit further includes a control device which controls the controllable input/output drivers.

15. An integrated circuit as claimed in claim 14, wherein the control device controls both the self-test circuit and the output circuit such that an initialization of the external circuit is performed in a first test cycle and the self test of the plurality of logic gates and the logic test of the external circuit are performed in a second test cycle.

16. An integrated circuit as claimed in claim 14, wherein the input/output circuit includes a bus connection for connecting to an external bus structure and the control device includes a bus control, wherein external circuit elements connected to the bus structure are selectively selected for a self-test via respective enable signals.

17. An integrated circuit as claimed in claim 16, wherein the bus control includes a counter for counting a bus clock signal, wherein the controllable input/output drivers are only selected during all even-numbered clock cycles of the bus clock signal and the respective enable signals are output sequentially during all odd-numbered clock signals of the bus clock signal for enabling the respective external circuit elements.

18. An integrated circuit as claimed in claim 10, wherein the input/output circuit can be selectively deactivated.